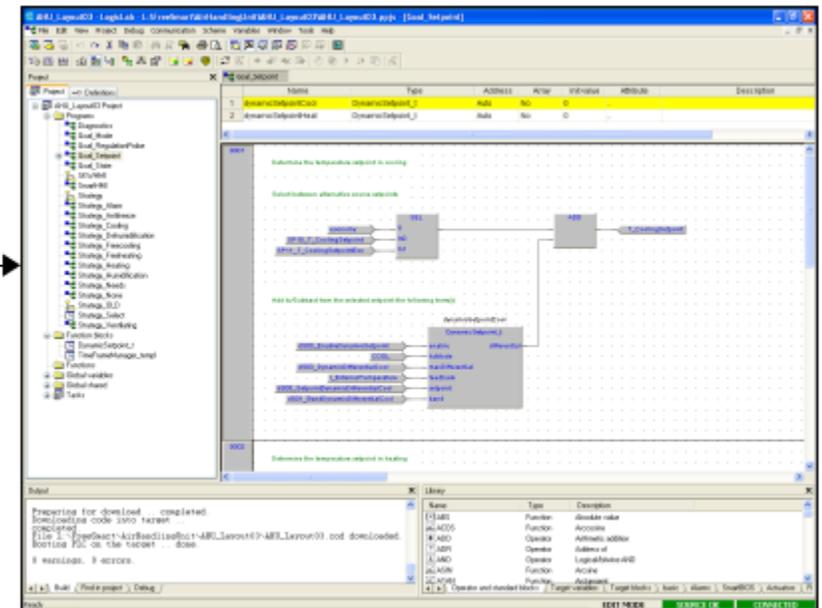
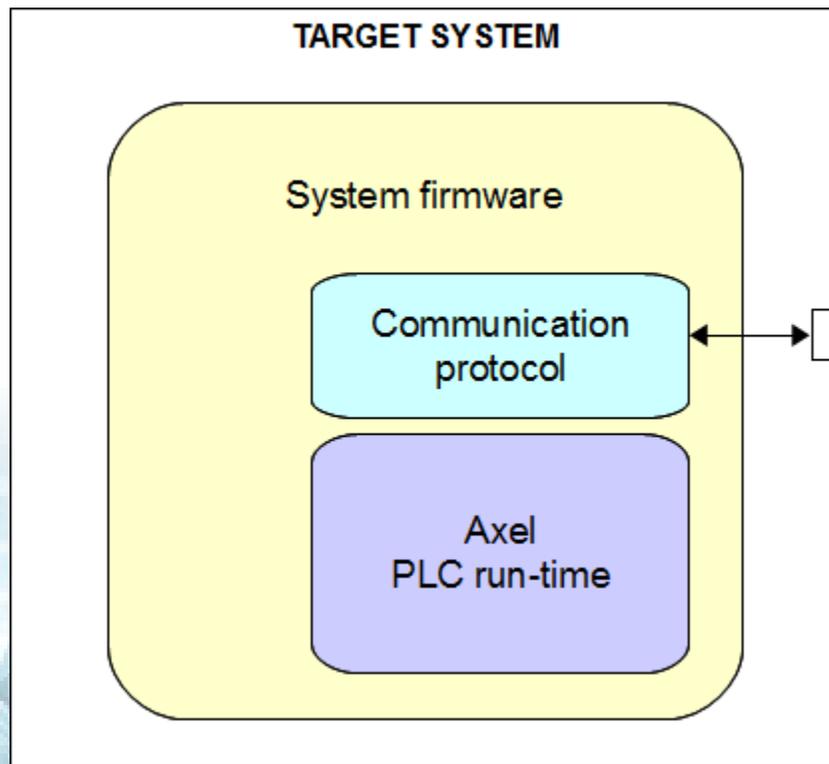


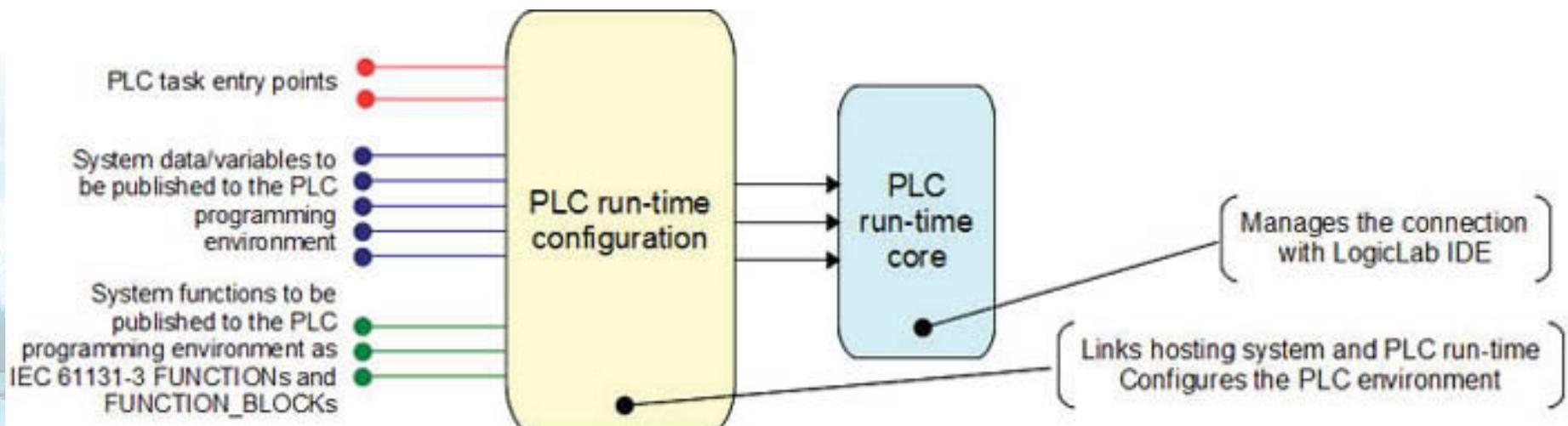
Program your product with LogicLab

In order to work with LogicLab, your product just needs Axel PLC run-time and generic network capabilities



The PLC run-time can be rapidly integrated into your product's software

- The PLC run-time building blocks are:
 - the run-time core, supplied as-is by Axel
 - the run-time configuration, adapted to meet system specific requirements
- Both are delivered as ANSI C programming language source code
- The run-time has to be linked into the firmware executable file, together with the rest of the system software



LogicLab can interface with any kind of communication hardware and software

- LogicLab already includes support for several standard communication protocols, including Modbus (both RTU and ASCII), CANopen, TCP/IP, and so on
- Custom communication protocols can be – and have been – used as well
- Protocol features required by the system are limited to:
 - Reading and writing simple objects (for example, Modbus registers or CANopen dictionary objects)
 - Reading and writing memory blocks
- The protocol can be extended to include missing features

There are no other system requirements

- No specific software architecture is needed: Axel PLC run-time adapts to the hosting environment, not viceversa
- Any operating system can host the PLC run-time and even no operating system at all is a choice
 - The run-time already proved to work on a full range of systems, from Microsoft Windows to real-time OS's, to very simple custom schedulers
- LogicLab works with virtually any hardware architecture and has been successfully ported on many 32-, 16-, and even 8-bit micro-controllers, including: ARM, Atmel AVR, Intel x86, Freescale ColdFire, Fujitsu 16LX/FX, Intel i960, Infineon TriCore, Infineon C166 and Texas Instruments TMS320

PLC run-time porting is done by our staff working closely with yours

- Most of the work required to port the PLC run-time onto your system is done by our software and system engineers
- We usually cooperate with at least one member of your engineering department working part-time to support Axel on topics related to your system, including:
 - supply of hardware and software tools required to work with your system
 - knowledge transfer, especially for custom parts of your system (for example, a custom communication protocol)
 - implementation of missing system functionalities
 - implementation of optional system-specific aspects of the PLC run-time

You come out with a complete IDE for your product, which you can easily maintain and further enrich

- As we deliver LogicLab to you, we provide you documentation and instructions on:
 - How to build your distribution package
 - How to customize the IDE (for example, to include your company name and logo)
 - How to maintain your product and create newer versions of it
 - How to develop and distribute libraries of IEC blocks and sample or real applications
- Moreover, LogicLab is highly customizable: including an embedded Web browser and a powerful scripting interface, the IDE can be extended with device-specific functionalities



- When porting starts, an Axcel technician is chosen as your preferred contact; after the porting is delivered, the same person still remains available for you
- We provide an effective Technical Support service, including an on-line tracking system
- As a consultancy and technology provider, Axcel will help you understand further needs related to your product, suggesting and/or supplying a solution

The screenshot shows a web browser window with the following elements:

- Browser tabs: O3Spaces - O3Spaces - Spaces, Custom Query - LogicLab
- LogicLab logo
- User: logged in as eliwell Logout
- Search bar: Wiki
- Table of tickets with columns: Ticket, Priority, Summary, Customer Version, Version, Type, Status, Resolution, Customer Fix Version, Fix Version

Ticket	Priority	Summary	Customer Version	Version	Type	Status	Resolution	Customer Fix Version	Fix Version
#596	critical	using variable associated with a datablock that use process image in a task without image process doesn't generate dynamic link record	2.0.4	2.12.0.7	defect	closed	fixed	2.0.x trunk	2.12.0.x trunk
#593	critical	With respect to Intel x86 architecture, MIN and MAX operations on unsigned 32-bit integer operand act as the operand were signed	2.0.4	2.12.0.6	defect	closed	fixed	trunk 2.0.x	trunk 2.12.0.7
#592	critical	If the output of an FBD block is directly connected to both the EN pin and another input of a following block, the compiler stops with an improper error	2.0.4	2.12.0.6	defect	closed	fixed	trunk 2.0.x	trunk 2.12.0.7
#590	critical	With respect to ARM architecture, the first valid value of input K of standard function MUX is 1: both the standard and the vast majority of other code generators require it to be 0	2.0.3	2.12.0.5	defect	closed	fixed	trunk 2.0.4	trunk 2.12.0.6
#589	critical	With respect to Intel x86 architecture, the first valid value of input K of standard function MUX is	2.0.3	2.12.0.5	defect	closed	fixed	trunk 2.0.4	trunk 2.12.0.6

We bet on your success: we earn as you profit from the new product

- Our business model reflects the will to develop partnerships rather than client/supplier relationships
- Once the PLC run-time porting phase is over, you purchase one license per product sold
 - The actual license price is tailored around your business and mainly depends on annual quantities
- LogicLab is free of charge: in order to use the IEC 61131-compliant IDE, neither a license nor a registration is required
- Porting price depends on your product technical specifications, but our business model helps to hold it down in order to reduce your initial investment